A single chip micro-nose

Diploma Thesis
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Overview

• The SMC
• Communication
• Testing - theory and setup
• Results
• Future improvements
• Conclusion
The SMC

- Analog+ digital
- \( I^2C \)-interface

Register bank

- Resistive heater
- Thermopile
- N-well island membrane
- Heating resistors
- Piezo-resistor
- Sensitive layer

- Capacitive
- Temperature

- Polymer
- Electrodes
- N-analyte
- Polarized analyte
- Substrate
- Air

Absorption, Polarization, Swelling
Communication for gas measurements

- enables us to do gas measurements (>10 h)
- initial timing problems were resolved by interrupt driven reception routines on PC and µC
- PC will be replaced by display and some keys for the handheld device
Testing - Why and What

Why?

- 6 SMCs are bonded onto a ceramic substrate
- we have to make sure that all of them are working

Requirements

- develop testing on a level that could be used for industrial application
- fast: about one second for each SMC
- automated: test a whole wafer

What to test?

- synchronous digital part: register bank, \(I^2C\) interface
- asynchronous counters (resonant and capacitive sensor)
- sensors and analog interface circuitry
Theory of (digital) testing

Fault models
- restriction to logic
- stuck-at model: signal is always L (sa0) or H (sa1)
- no bridges, no time-dependent faults, no clustering of faults

Controllability, observability
an internal node is
- controllable, if we can find a stimulus that forces it to be either L or H
- observable, if there is a specific output pattern that unequivocally indicates its state

What to do
- synthesize stimuli and correct answers: ATPG
- apply stimuli
- compare the logic’s output to computed answers
The scan chain

Problems so far:
• sequential logic not testable
• too many pads needed

Scan chain
• all flip flops form a shift register
• access to all internal flip flops
• asynchronous counters still not testable
Mixed signal testing

Problems
- analog circuitry is ‘hidden’: SMC has only digital pins
- cannot perform standard analog tests (power consumption, voltage measurement..)
- no simple fault model like the stuck-at model available for analog

Solution
- try to isolate blocks as far as possible
- develop testing schemes that use digital blocks (counters, filters, I²C, scan chain - all tested before) to perform tests on analog circuits
- even then, sensor output not controllable -> include additional testing features already in design phase
Setup

ATPG, Analog test

Perl scripts

Agilent format

PCB

Agilent format

Perl scripts

Results

Agilent 16702
Digital test

- 880,000+ lines are tested @ 1 MHz, but current generator card can only do 256k -> split
- If the output file is empty, no errors were detected
Asynchronous counter test

• Not testable in scan chain, as they are like scan chains by themselves
• Idea: set them to their maximum value from which they count down, operate them in non-test mode for a specified number of clock cycles (in our case 524’288), and check if they trigger at the right time
• Problem: clock divider at the clock input -> not 524’288, but 134e6 clocks needed -> way too many for the generator
• Can be replaced by synchronous counters which are scan path testable, but 20% bigger
Sensor test

**Capacitive sensor**
- step through parameters in register bank and watch the output
- limiting factor for testing time: gate time. 64 steps -> don’t test all

**Calorimetric sensor**
- analog and digital filter form a lowpass -> turn on heater and read filter output
- use scan chain or I²C interface
- fast: one value every millisecond

**Resonant sensor**
- hard to test: feedback loop is ‘hidden’
- scan parameter space for stable region
- takes about 6.5 s

**Temperature sensor**
- heat prober chuck
Results and challenges

• communication over the I²C interface works well
• gas measurements have been successfully performed
• digital and analog test setup works
• testing the 1\textsuperscript{st} generation SMC shows problems -> mask redesign
  • n-well has to be connected to vdd potential for resonant sensor -> whole waver acts as a diode (etch stop network)
• sensor input not set to 0 for digital test
• 2\textsuperscript{nd} waver run just arrived, tests have to be performed
• Agilent 16702 still has some (software) problems that are addressed in cooperation with Agilent
Improvements

Asynchronous counter
- bypass clock divider for gate time counter
- use external counter for long sequences in non-testing mode

Resonant sensor
- delay line hidden so far
- \(\Delta t\) create feedback loop \(\Rightarrow\) measure oscillator frequency

Calorimetric sensor
- chopper frequency unknown
- \(\Delta t\) connect it to counter
Conclusion

• set up communication SMC - µC - PC
• met requirements to develop test setup to test SMC in few seconds
• wrote converters to translate test vectors from design tool to Agilent Logic Analyzer format that can easily be adapted for future testing purposes
• wrote additional scripts and read-out programs
• performed first tests
• developed improvements for next design
• made first gas measurements